

WHAT IS CLAIMED IS:

1 1. A system comprising:

2 a GPS receiver module adapted to extract clock information and time of date(TOD)
3 information from a received GPS signal, to generate a first clock signal and first TOD data, and
4 to output the first clock signal and first TOD data to a first base transceiver station and a base
5 transceiver station of a next stage, the GPS receiver module being arranged within the first
6 base-station transceiver; and

7 a clock module adapted to generate a second clock signal and second TOD data
8 synchronized with the first clock signal and first TOD data by performing a delay correction with
9 one of the GPS receiver module of the first base transceiver station or a base transceiver station
10 of a previous stage, and to output the second clock signal and second TOD data to its base
11 transceiver station and a base transceiver station of the next stage upon the clock module receiving
12 a first clock signal and first TOD data from one of the GPS receiver module of the first base
13 transceiver station or the base transceiver station of the previous stage, the clock module being
14 arranged within a base transceiver station other than the first base-station transceiver.

1 2. The system according to claim 1, wherein the GPS receiver module comprises:

2 a GPS engine adapted to extract the clock information and TOD information from the
3 received GPS signal;

4 a PLL module adapted to generate the first clock signal and first TOD data according to the

5 extracted clock information and TOD information;

6 a driver adapted to output the first clock signal and first TOD data to the first base
7 transceiver station and the base transceiver station of the next stage;

8 a return module adapted to effect delay correction by returning a delay correction signal
9 received from a clock module of the base transceiver station of the next stage; and

10 a processor adapted to control extracting clock information and TOD information with the
11 GPS engine, to control generating a first clock signal and first TOD data with the PLL module, to
12 control outputting the first clock signal and first TOD data to its base transceiver station and the
13 base transceiver station of the next stage, and to control processing a delay correction request
14 received from the base transceiver station of the next stage with the return module, upon the
15 processor receiving the GPS signal from the GPS antenna.

1 3. The system according to claim 1, wherein the clock module comprises:

2 a delay correction module adapted to receive the clock signal and the TOD data from one
3 of the first base transceiver station or the base transceiver station of the previous stage, to measure
4 a delay of the received clock, and to generate a delay correction value;

5 a PLL module adapted to receive the clock signal and the TOD data received in the delay
6 correction module and the delay correction value and to generate a second clock signal and second
7 TOD data corrected in accordance with the delay correction value;

8 a driver adapted to output the second clock signal and second TOD data to its base
9 transceiver station and the base transceiver station of the next stage;

10 a return module adapted to effect delay correction by returning the delay correction signal
11 received from a clock module of the base transceiver station of the next stage; and

12 a processor adapted to control performing a delay correction of the clock signal and the
13 TOD data received from one of the first base transceiver station or the base transceiver station of
14 the previous stage with the delay correction module and the PLL module, to control outputting the
15 second clock signal and second TOD data to its base transceiver station and the base transceiver
16 station of the next stage using the driver, and to control processing of a delay correction request
17 received from the base transceiver station of the next stage with the return module.

1 4. The system according to claim1, wherein the delay correction module is adapted to
2 measure the delay of the clock received in the GPS receiver module of one of the first base
3 transceiver station or the base transceiver station of the previous stage by transmitting the delay
4 correction signal to one of the GPS receiver module of the first base transceiver station or the base
5 transceiver station of the previous stage, and to measure and correct the delay in accordance with
6 a signal returned thereto.

1 5. A system comprising:

2 a main base transceiver station having a GPS receiver module adapted to extract clock
3 information and TOD information from a received GPS signal and to generate a clock signal and
4 TOD data used for operating its base-station transceiver; and

5 at least one sub-base transceiver station, each at least one sub-base transceiver station

6 having a clock module adapted to receive a clock signal and TOD data from one of the GPS
7 receiver module of the main base transceiver station or an adjacent base transceiver station through
8 a daisy chain, and to generate a clock signal and TOD data synchronized with the clock signal and
9 the TOD data used in the main base transceiver station by performing a delay correction with one
10 of the GPS receiver module which has transmitted the clock signal and the TOD data or the
11 adjacent base-station transceiver.

1 6. A method comprising:

2 extracting clock information and TOD information from a received GPS signal, with a first
3 base transceiver station having a GPS receiver module;

4 outputting a clock signal and TOD data used for operating the first base transceiver station
5 from the extracted clock information and TOD information from the first base-station transceiver;

6 receiving clock signals and TOD data from one of the first base transceiver station or a base
7 transceiver station of the previous stage through a daisy chain, with a base transceiver station other
8 than the first base-station transceiver;

9 measuring and correcting delays of the received clock signals and TOD data with a base
10 transceiver station other than the first base-station transceiver; and

11 generating clock signals and TOD data synchronized with the clock signal and the TOD
12 data used in the first base transceiver station by reflecting a value of the delay correction to the
13 received clock signals and TOD data, and outputting the synchronized clock signals and TOD data
14 to its base transceiver station and the base transceiver station of the next stage, with a base

transceiver station other than the first base-station transceiver.

7. The method according to claim 6, wherein measuring and correcting the delay includes transmitting the delay correction signal to one of the first base transceiver station or the base transceiver station of the previous stage, and measuring and correcting a delay using a signal being returned, in order to measure a clock delay received from one of the first base transceiver station or the base transceiver station of the previous stage.

8. A system comprising:
a first base transceiver station including a GPS receiver module adapted to extract clock information and time of date (TOD) information from a received GPS signal and to generate and output a clock signal and TOD data therefrom; and
another base transceiver station including a clock module, the clock module being coupled to the GPS receiver module of the first-base transceiver station and adapted to receive the clock signal and TOD data from the GPS receiver module and to generate another clock signal and another TOD data synchronized with the clock signal and TOD data from the GPS receiver module by performing a delay correction.

9. The system of claim 8, further comprising at least one other base transceiver station including another clock module, the another clock module being coupled to the clock module of the another base transceiver station and adapted to receive the clock signal and TOD data from the

4 another clock module and to generate an additional clock signal and an additional TOD data
5 synchronized with the clock signal and TOD data from the another clock module by performing
6 a delay correction.